

**Appl. No. : 09/643,636**  
**Filed : August 22, 2000**

### **REMARKS**

The following remarks are responsive to the April 19, 2004 Final Office Action.

#### **Status of the Claims**

Claims 1-7, 9-17, 22 and 24-29 are pending in this application. No amendments are requested in this paper. Thus, Claims 1-7, 9-17, 22 and 24-29 are presented for further consideration as previously presented in Applicants' response to the previous Office Action.

#### **Summary of the April 19, 2004 Final Office Action**

In the Final Office Action, the Examiner allows Claim 29. The Examiner rejects Claims 1-7, 9-17, 22 and 24-28.

The Examiner rejects Claims 1-3, 5, 9-11 and 24-28 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,381,659 to Proch et al. ("Proch") in view of U.S. Patent No. 6,490,635 to Holmes ("Holmes").

The Examiner rejects Claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Holmes in view of Proch or Applicants' admitted prior art and in further view of Official Notice taken by the Examiner.

The Examiner rejects Claims 4, 6-7 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Proch in view of Holmes and in further view of Official Notice.

The Examiner rejects Claims 24-27 under 35 U.S.C. § 103(a) as being unpatentable over Holmes in view of Proch or Applicants' admitted prior art.

The Examiner rejects Claims 13-17 under 35 U.S.C. § 103(a) as being unpatentable over Holmes in view of Proch or Applicants' admitted prior art and in further view of Official Notice and in further view of U.S. Patent No. 5,729,718 to Au ("Au").

For the reasons presented below, Applicants respectfully submit that Claims 1-7, 9-17, 22 and 24-28 are in condition for allowance along with presently allowed Claim 29.

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**Allowable Subject Matter—Claim 29**

Applicants thank the Examiner for the indication of allowable subject matter in independent Claim 29.

**Response to Claim Rejections Under 35 U.S.C. § 103(a)**

**Claims 1–3, 5 and 9–11**

The Examiner rejects independent Claim 1 as being unpatentable over Proch in view of Holmes. For the reasons set forth below, Applicants respectfully submit that Claim 1 and dependent Claims 2–3, 5 and 9–11 are patentably distinguished over the cited references.

**Address Registers Identify Locations in Buffer Memory**

Among other limitations, Claim 1 recites a buffer memory controller comprising a data buffer and a plurality of address registers. The data buffer is configured to buffer write operation data between a buffer memory and a write head of a disk. Each address register is configured to store an address, or location, of write operation data stored in a buffer memory.

Neither Proch nor Holmes nor any combination of Proch and Holmes teaches or suggests a buffer memory controller as recited in Claim 1. In particular, as discussed on page 17 of Applicants' Amendment filed on February 6, 2004, neither cited reference teaches a buffer memory controller having address registers configured to store addresses of write operation data stored in a buffer memory.

Proch appears to disclose a method and circuit for controlling a first-in first-out ("FIFO") buffer such that the buffer can accommodate multiple data blocks without overlapping data between adjacent data blocks. The Examiner cites Figure 2 of Proch for disclosing a data buffer (FIFO Buffer 144) between a buffer memory (RAM Buffer 25) and a write head of a disk (31, 32). The Examiner also cites Figure 2 of Proch as disclosing address registers (148, 152a-b and 154a-b) that "identify location[s] of write operation data stored within the buffer memory" (see page 3 of Final Office Action).

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Applicants respectfully traverse the Examiner's stated basis for the rejection because the registers of Proch do not store addresses identifying locations of data stored within the buffer memory (RAM Buffer 25) in accordance with the limitation recited in Claim 1. Unlike the claimed invention, the registers of Proch are configured to store the beginning addresses and ending addresses of data stored in the data buffer (FIFO Buffer 144) (see column 6 at line 47 through column 7 at line 22). The FIFO Buffer 144 and the RAM buffer 25 in Proch are distinct elements and have different structures and functions. The storage of the addresses of the FIFO buffer 144 does not in any manner correspond to the storage of the addresses in the buffer memory defined in Claim 1 of the present application. Contrary to the Examiner's statements, the structure defined in Claim 1 is not found in Proch. Therefore, Proch can not be combined with Holmes in the manner suggested by the Examiner in order to produce the invention defined in Claim 1.

In view of the foregoing, Applicants respectfully submit that neither Proch nor Holmes nor any combination of Proch and Holmes teaches a buffer memory controller having address registers configured to store addresses of write operation data stored in a buffer memory.

#### **Single Command for Out of Order Execution of Multiple Write Operations**

Claim 1 also defines the buffer memory controller as having controller logic configured to transfer, based on a single command, the data of at least two write operations in an order other than the order in which the two write operations were received by the buffer memory. This allows for out-of-order execution of write operations wherein the data of multiple write operations is transferred in response to a single command from a processor. For example, in one embodiment of the claimed invention, the two write operations can be executed out of order during a single revolution of the hard disk.

The Examiner cites Proch (column 10 at line 60) for disclosing controller logic configured to transfer, from the buffer memory to the data buffer, the data of at least two write operations based upon a single command to the controller logic. However,

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Proch does not provide any teaching or suggestion of such controller logic. Rather, Proch appears to disclose the writing of multiple data blocks to the data buffer (FIFO Buffer 144) rather than the transfer of data from multiple write operations. Proch does not teach or suggest that each of the multiple data blocks stored in the data buffer corresponds to a single write operation.

Holmes is directed to a conflict detection method for a disk drive controller. In particular, Holmes discloses a method for restricting the reordering of commands if there is an address range overlap between a newly received write command and other queued commands (read or write). Holmes also does not appear to teach the transfer of data from multiple write operations based on a single command to the controller logic.

In view of the foregoing, Applicants respectfully submit that neither Proch nor Holmes nor any combination of Proch and Holmes, teaches controller logic configured to transfer, based on a single command, the data of at least two write operations in an order other than the order in which the two write operations were received by the buffer memory.

#### **Summary of Discussion of Claim 1**

For at least the foregoing reasons, Applicants respectfully submit that no combination of Proch and Holmes teaches or suggests the invention defined in Claim 1. Therefore, Claim 1 is patentably distinguished over the cited references. Applicants respectfully request the Examiner to withdraw the rejection of Claim 1 and to pass Claim 1 to allowance.

#### **Dependent Claims 2-3, 5 and 9-11**

Claims 2-3, 5 and 9-11 depend from independent Claim 1 and further define the invention defined in Claim 1. Claims 2-3, 5 and 9-11 are patentably distinguished over the cited references for at least the reasons set forth above with respect to the patentability of Claim 1. Claims 2-3, 5 and 9-11 are further patentably distinguished over the cited references in view of the additional limitations recited in Claims 2-3, 5 and 9-11. Applicants respectfully request allowance of Claims 2-3, 5 and 9-11.

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### **Claims 24–27**

The Examiner rejects independent Claim 24 as being unpatentable over Proch in view of Holmes. The Examiner also rejects Claim 24 as being unpatentable over Holmes in view of Proch or Applicants' admitted prior art. For the reasons set forth hereafter, Applicants respectfully submit that Claim 24 and dependent Claims 25–27 are patentably distinguished over the cited references.

Among other limitations, Claim 24 recites receiving in a different one of a plurality of address registers an address, within a buffer memory, of write operation data for each of a plurality of write operations. A single command is received to provide the write operation data of a plurality of write operations. The data of the plurality of write operations is then written in an order other than the order in which the data of each of the write operations was received in the buffer memory.

Neither Proch nor Holmes nor any combination of Proch and Holmes teaches or suggests the method recited in Claim 1. In particular, neither cited reference teaches receiving in each of a plurality of address registers an address, within a buffer memory, of write operation data of a plurality of write operations. In addition, neither cited reference teaches receiving a single command to provide the data of the plurality of write operations and writing the data in an order other than the order in which the data was received by the buffer memory.

As previously discussed with respect to Claim 1, Proch does not disclose the use of a plurality of address registers to store a location of data in a buffer memory. The address registers of Proch store the beginning addresses and ending addresses of data stored in a first-in first-out buffer (FIFO Buffer 144), which the Examiner identifies as a "data buffer." Even if the FIFO Buffer 144 is considered a "buffer memory," the data stored in the FIFO Buffer 144 is always provided to be written in the same order, which is the order in which the data was received by the FIFO Buffer 144. Thus, Proch does not teach or suggest a method including the writing of data from a plurality of write operations in an order other than the order in which the data was received at the buffer memory.

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Furthermore, as discussed above with respect to Claim 1, the portions of Proch cited by the Examiner do not teach or suggest receiving a single command to provide the write operation data of a plurality of write operations.

Proch cannot properly be combined with Holmes to teach or suggest the method recited in Claim 1. Holmes discloses a method of detecting conflicts resulting from the reordering of commands by a disk drive controller. The method of Holmes cannot be properly combined with the method of Proch because the FIFO Buffer 144 of Proch requires that data stored in the FIFO Buffer 144 be provided in the same order that the data was received by the FIFO Buffer 144. Attempting to modify the method in Proch to allow for out-of-order execution of data stored in the FIFO Buffer 144 would inappropriately modify the Proch invention by rendering the invention unsatisfactory for its intended purpose. In addition, the address registers of Proch would have to be modified to provide a wholly different function than that of their intended function of capturing and saving addresses of data blocks in the FIFO Buffer 144 such that the data blocks do not overlap each other. See M.P.E.P. 2143.02 ("If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.")

Applicants' specification states generally that prior art discloses that two write commands can be combined into a single write command. However, Applicants submit that this general statement in combination with the other cited references still does not teach or suggest each element of the method of Claim 24.

For at least the foregoing reasons, Applicants respectfully submit that no combination of Proch and Holmes and Applicants' admitted prior art teaches or suggests the invention defined in Claim 24. Therefore, Claim 24 is patentably distinguished over the cited references. Applicants respectfully request the Examiner to withdraw the rejection of Claim 24 and to pass Claim 24 to allowance.

Claims 25–27 depend from independent Claim 24 and further define the invention defined in Claim 24. Claims 25–27 are patentably distinguished over the cited references for at least the reasons set forth above with respect to the patentability of

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Claim 24. Claims 25–27 are further patentably distinguished over the cited references in view of the additional limitations recited in Claims 25–27. Applicants respectfully request allowance of Claims 25–27.

#### **Claim 28**

The Examiner rejects independent Claim 28 as being unpatentable over Proch in view of Holmes.

Independent Claim 28 includes features that are similar to limitations of Claim 1. Claim 28 also includes other limitations in combination with the previously discussed limitations. Applicants respectfully submit that Claim 28 is patentably distinguished over the cited references for reasons set forth above with respect to Claim 1. Claim 28 is further patentably distinguished over the cited references in view of the additional combination of limitations defined in Claim 28.

#### **Claim 12**

The Examiner rejects Claim 12 as being unpatentable over Holmes in view of Proch or Applicants' admitted prior art (in particular, pages 1–2 of Applicants' specification) and in further view of Official Notice. For the reasons set forth below, Applicants respectfully submit that Claim 12 is patentably distinguished over the cited references.

Independent Claim 12 includes features that are similar to limitations of Claim 24. Applicants respectfully submit that Claim 12 is patentably distinguished over the cited references for reasons set forth above with respect to Claim 24. Claim 12 also includes other limitations in combination with the previously discussed limitations. Thus, Claim 12 is further patentably distinguished over the cited references in view of the defined combination of limitations.

Applicants note that the Examiner has taken Official Notice in this Final Office Action and in the previous Office Action. In particular, the Examiner states on page 7 of the Final Office Action:

[B]oth the concept and the advantages of providing a disk formatter are well known in the art. It would have been obvious to one of ordinary skill

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in the art at the time the invention was made to provide for a disk formatter because it would allow address or block count to be access[ed] in the same order as received and data to be processed in a predetermined format.

Applicants note that disk formatters are known in the art. However, not all concepts and advantages are provided by all disk formatters, and novel and non-obvious developments in the field of disk formatters are not precluded by the mere existence of disk formatters. The Examiner's assertion of Official Notice that disk formatters exist without citing the teaching of any feature of a particular formatter with respect to the claimed invention does not support the Examiner's rejection of Claim 12.

Applicants respectfully submit that Claim 12 is patentably distinguished over the cited references because the cited references do not teach or suggest the recited combination of limitations in Claim 12. Applicants respectfully request allowance of Claim 12.

#### **Claim 4 and 6-7**

The Examiner rejects Claims 4 and 6-7 as being unpatentable over Proch in view of Holmes and in further view of Official Notice.

Claims 4 and 6-7 depend from independent Claim 1 and further define the invention defined in Claim 1. Claims 4 and 6-7 are patentably distinguished over the cited references for at least the reasons set forth above with respect to the patentability of Claim 1. Claims 4 and 6-7 are further patentably distinguished over the cited references in view of the additional limitations recited in Claims 4 and 6-7.

Applicants note that the Examiner takes Official Notice that:

[B]oth the concept and the advantages of providing . . . block count registers as FIFO, disk formatter, or address registers as FIFO are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide . . . a block count register as FIFO, providing data to a disk formatter, or address registers as FIFO because it would allow address or block count to be access[ed] in the same order as received and data to be processed in a predetermined format.



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Applicants note that block count registers, disk formatters, and address registers are known in the art. However, not all concepts and advantages are provided by all block count registers, disk formatters and address registers, and novel and non-obvious developments with respect to these elements and combinations of the elements are not precluded by the mere existence of the elements. The Examiner's assertion of Official Notice that block count registers, disk formatters and address registers exist without citing the teaching of any feature of a particular block count register, disk formatter or address register with respect to the claimed invention does not support the Examiner's rejection of Claims 4 and 6-7.

Applicants respectfully submit that Claims 4 and 6-7 are patentably distinguished over the cited references because the cited references do not teach or suggest the recited combination of limitations in Claims 4 and 6-7. Applicants respectfully request allowance of Claims 4 and 6-7.

#### **Claim 22**

The Examiner rejects Claim 22 as being unpatentable over Proch in view of Holmes and in further view of Official Notice.

Independent Claim 22 includes features that are similar to limitations of Claim 24. Applicants respectfully submit that Claim 22 is patentably distinguished over the cited references for the reasons set forth above with respect to Claim 24. Claim 22 includes other limitations in combination with the previously discussed limitations. The cited references do not teach or suggest the recited combination of limitations in Claim 22. Furthermore, for the reasons discussed above, Applicants respectfully submit that the Official Notice taken by the Examiner with respect to the general existence of disk formatters in the prior art does not support the rejection of Claim 22.

In view of the foregoing, Applicants respectfully submit that Claim 22 is patentably distinguished over the cited references, and Applicants respectfully request allowance of Claim 22.

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### **Claims 13-17**

The Examiner rejects Claims 13-17 as being unpatentable Holmes in view of Proch or Applicants' admitted prior art and in further view of Official Notice and in further view of Au.

Claims 13-17 depend from independent Claim 12 and further define the invention defined in Claim 12. Claims 13-17 are patentably distinguished over the cited references for at least the reasons set forth above with respect to the patentability of Claim 12. Claims 13-17 are further patentably distinguished over the cited references in view of the additional limitations recited in Claims 13-17. Applicants respectfully submit that Claims 13-17 are patentably distinguished over the cited references, and Applicants respectfully request allowance of Claims 13-17.

### **Summary**

In view of the foregoing amendments and the foregoing remarks, Applicants respectfully submit that the present application is now in condition for allowance, and Applicants respectfully request allowance of Claims 1-3, 5, 9-11, 22 and 24-28 in addition to presently allowed Claim 29.

### **Request for Telephone Interview to Resolve Any Remaining Issues**

If further issues remain to be resolved after consideration of this paper, Applicants respectfully request the Examiner to call Applicants' undersigned attorney of record at 949-721-2849 or at the general office number listed below.

Respectfully submitted,  
KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: JUNE 16, 2004

By: Jerry T. Sewell  
Jerry T. Sewell  
Registration No. 31,567  
Attorney of Record  
Customer No. 20,995  
(949) 760-0404